DUAL DAMASCENE PROCESS FOR FORMING A MULTI-LAYER LOW-K DIELECTRIC INTERCONNECT

ABSTRACT OF THE DISCLOSURE

In a dual damascene process for forming a multi-layer low-k dielectric interconnect, the formation of each layer of interconnect comprises deposition of a first low-k dielectric layer, etching of the first low-k dielectric layer to form two dual damascene vias, formation of two Cu conductor plugs enclosed with barrier layers in the two dual damascene vias, etching of the first low-k dielectric layer between the two dual damascene vias to form a trench, and spin-on of a second low-k dielectric layer filled in the trench. The spin-on low-k dielectric layer is selected to have a dielectric constant smaller than that of the first low-k dielectric layer to reduce the equivalent dielectric constant in the layer of interconnect.